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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,730	07/31/2003	Joseph C. Fjelstad	SIPI-P110	3880

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,730	FJELSTAD ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16 and 19-23* is/are allowed.

6)☐ Claim(s) *1,2,4-10,12,13 and 17* is/are rejected.

7)☒ Claim(s) *3,11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-23** are pending in this application, which claims benefit of 60/400,298 filed 07/31/2002, is acknowledged.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 2, 4-10, 12, 13 and 17** are rejected under 35 U.S.C. 102(b) as being anticipated by Iadarola et al. (USP: 4,543,715 hereinafter referred to as "Iadarola").

Regarding claim **1**, Iadarola discloses in Fig. 1 and the corresponding texts as set forth in column 2, line 1-column 3 line 4, a multilayered circuit component/a multilayer printed circuit board (10) comprises:

two or more layers (13);

a first surface of the two or more layers upon which a first plurality of circuit paths (31-35) are provided;

a second surface of the two or more layers upon which a second plurality of circuit paths (31-35) are provided;

an aperture extending through at least a portion of the two or more layers, the aperture being defined by a first opening (59) on the first surface, a second opening (59) on the second surface, and an internal surface of the two or more layers that extends between the first surface and the second surface;

a first trace element/a first vertical circuit trace (51) provided over a portion of the internal surface of the aperture to expend between the first surface and the second surface, the first trace element extending onto the first surface to form a first partial perimeter of the first opening;

wherein the first trace element/the first vertical circuit trace is formed by plating a first hole/opening (59) on the first surface, and then subsequently forming the aperture to intersect the first hole, so that after the aperture is formed, a remaining portion of the first hole/opening has plating that forms the first trace element.

Regarding claim **2**, Iadarola discloses in Fig. 1 the component wherein the multilayered circuit component/the multilayer printed circuit board further comprises:

a second trace element/a second vertical circuit trace (52) provided over a portion of the internal surface of the aperture to extend between the first surface and the second surface, the second trace element extending onto the first surface to form a second partial perimeter of the first opening; and

wherein the first trace element/the first vertical circuit trace and the second trace element/the second vertical circuit trace are formed by plating the first hole and a second hole on the first surface, and then subsequently forming the aperture to intersect the first hole and the second hole, so that after the aperture is formed, the remaining portion of the first hole has

plating that forms the first trace element/the vertical circuit trace, and a remaining portion of the second hole has plating that forms the second trace element/the vertical circuit trace.

Regarding claims **4-5**, Iadarola discloses in Fig. 1 the component wherein at least one of the first surface or the second surface is a grounding plane; wherein at least one of the first surface or the second surface is a power plane.

Regarding claims **6-7 and 12**, Iadarola discloses in Figs. 1-2 the component wherein the aperture has an irregular cross-section (Fig. 2), and wherein each of the first trace element/the first vertical circuit trace and the second trace element/the second vertical circuit trace is rounded as it extends on the internal surface of the aperture.

Regarding claims **8-10**, Iadarola discloses in Figs. 1-2 the component wherein the component forms part of a backplane; wherein the first trace element/the first vertical circuit trace has a radius of curvature that defines a corresponding circle, wherein the first trace element/the first vertical circuit trace has an arc length that is less than 50% of a circumference of the corresponding circle; and wherein the arc length of the first trace element/the first vertical circuit trace is less than 33% of the circumference of the corresponding circle.

Regarding claim **13**, Iadarola discloses in Fig. 2 the component wherein a cross-section of the aperture is shaped to have a plurality of different radii of curvatures.

Regarding claim **17**, Iadarola discloses in Figs. 1-2 and the corresponding texts as set forth in column 2, line 1-column 3 line 4, a multilayered circuit component/a multilayer printed circuit board (10) comprises:

two or more layers (13);

a first surface of the two or more layers upon which a first plurality of circuit paths (31-35) are provided;

a second surface of the two or more layers upon which a second plurality of circuit paths (31-35) are provided;

an aperture extending through at least a portion of the two or more layers, the aperture being defined by a first opening (59) on the first surface, a second opening (59) on the second surface, and an internal surface of the two or more layers that extends between the first surface and the second surface;

a first trace element/a first vertical circuit trace (51) provided over a first portion of the internal surface of the aperture to extend between the first surface and the second surface, the first trace element/the first vertical circuit trace being rounded and extending onto the first surface to form a first partial perimeter of the first opening;

a second trace element/a second vertical circuit trace (52) provided over a second portion of the internal surface of the aperture to extend between the first surface and the second surface, the second trace element being rounded and extending onto the second surface to form a second partial perimeter of the first opening;

wherein the opening of the aperture has a plurality of radii of curvatures (Fig. 2).

Allowable Subject Matter

Claims **3, 11 and 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the

applicant's disclosure does not teach or suggest the claimed limitations. Iadarola fails to teach the claimed limitation the component wherein the first trace element and the second trace element each form a pedal shaped support element on the first surface as recited in claim **3**; the component wherein the first trace element has a radius of curvature that defines a first circle, the second trace element has a radius of curvature that defines a second circle, and wherein the first trace element and the second trace element each have an arc length that is less than 50% of a circumference of the corresponding first or second circle as recited in claim **11**; the component wherein the first partial perimeter of the first opening has a first radius of curvature, the second partial perimeter of the first opening has a second radius of curvature, and another perimeter portion of the opening has a third radius of curvature, wherein at least the third radius of curvature is different than the first radius of curvature and the second radius of curvature as recited in claim **18**;.

Claims **14-16 and 19-23** are allowed. The following is a statement of reason for the indication of allowable subject matter: Claims **14-16 and 19-23** are considered allowable since the prior art made of record and considered pertinent to the application's disclosure does not teach or suggest the claimed limitations. Iadarola fails to teach the claimed limitations a multilayered circuit component comprises each aperture is shaped to receive a corresponding male connector element that can extend into the aperture and make electrical contact with the one or more trace elements that are provided in that aperture, so that another layer comprising an array of male connectors is matable with the component using the array of apertures of the surface as recited in independent claim **14**, and a multilayered circuit component comprises a plurality of trace element clusters, each trace element cluster extending inward from the first

surface of the first layer to an other surface of the multi-surfaced circuit component, wherein each trace element cluster includes at least (i) a first trace element for providing a first connection to one or more current bearing components on the other surface that the first trace element extends to, and (ii) a second trace element for providing a second connection to one or more current bearing components on the other surface that the second trace element extends to as recited in independent claim **19**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ah

09/09/04

Andy Huynh

Patent Examiner